What is claimed is:

1. A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

2. A method according to claim 1, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

3. A method according to claim 2, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

4. A method according to claim 1, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of

said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

5. A semiconductor device manufactured by a method according to claim 1, said semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, wherein said second nitride film is formed in at least a portion of the surface of the semiconductor substrate in said low-density region.

6. A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes and also expose said nitride protective films on said gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said first nitride film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes

reaching said semiconductor substrate in said interlayer insulating film;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

7. A method according to claim 6, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

8. A method according to claim 7, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

9. A method according to claim 6, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the

atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

10. A semiconductor device manufactured by a method according to claim 6, said semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, wherein said second nitride film is formed in at least a portion of the surface of the semiconductor substrate in said low-density region.

11. A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming oxide films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

masking said high-density region of said semiconductor substrate, and etching said first nitride film in only said low-density region to expose said gate oxide film in gaps between said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes in said low-density region;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes reaching said semiconductor substrate in said interlayer insulating film;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

12. A method according to claim 11, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

13. A method according to claim 11, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

14. A method according to claim 11, wherein said first nitride film is formed by a chemical vapor deposition process, and said second nitride film is formed by a rapid thermal nitriding process.

15. A method according to claim 14, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm.

16. A method according to claim 11, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film

is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

17. A semiconductor device manufactured by a method according to claim 11, said semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, wherein said second nitride film is formed in at least a portion of the surface of the semiconductor substrate in said low-density region.

18. A method of manufacturing a semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, comprising the steps of:

forming a gate oxide film on a surface of said semiconductor substrate;

forming gate electrodes on a surface of said gate oxide film, and forming nitride protective films on said gate electrodes;

uniformly forming a first nitride film having a predetermined thickness on the surface with the gate electrodes formed thereon;

etching said first nitride film to expose said gate oxide film in gaps between said gate electrodes and also expose said nitride protective films on said gate electrodes;

etching the exposed gate oxide film to expose said semiconductor substrate in the gaps between gate electrodes;

uniformly forming a second nitride film having a predetermined thickness on the surface on which said gate oxide film is etched;

forming an interlayer insulating film with an impurity introduced therein on a surface of said second nitride film;

annealing an assembly formed so far in an atmosphere containing water vapor;

self-aligning said high-density region using said first nitride film positioned on sides of said gate electrodes as an etching stopper to form contact holes

reaching said semiconductor substrate in said interlayer insulating film;

forming contact electrodes connected to said semiconductor substrate in said contact holes; and

annealing an assembly formed so far with a forming gas to recover an interfacial level.

19. A method according to claim 18, wherein said first nitride film and said second nitride film are formed by a chemical vapor deposition process.

20. A method according to claim 18, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 3.0 to 20 nm.

21. A method according to claim 18, wherein said first nitride film is formed by a chemical vapor deposition process, and said second nitride film is formed by a rapid thermal nitriding process.

22. A method according to claim 21, wherein said first nitride film is formed to a thickness ranging from 30 to 50 nm, and said second nitride film is formed to a thickness ranging from 1.8 to 2.0 nm.

23. A method according to claim 18, wherein said first nitride film is formed to a thickness large enough to serve as an etching stopper for self-aligning said high-density region, and said second nitride film is formed to a thickness which prevents an impurity of said interlayer insulating film from being diffused into said semiconductor substrate by annealing the assembly in the atmosphere containing the water vapor and also prevents said semiconductor substrate from being oxidized by annealing the assembly in the atmosphere containing the water vapor, but allows said forming gas to be diffused into said semiconductor substrate.

24. A semiconductor device manufactured by a method according to claim 18, said semiconductor device having, on a single semiconductor substrate, a high-density region containing transistor elements arrayed at a high density and a low-density region containing transistor elements arrayed at a low density, wherein said second nitride film is formed in at least a portion of the surface of the semiconductor substrate in said low-density region.